REMARKS

Claims 1 through 21 are pending. Claims 1, 8, and 15 have been amended. New claim 21 has been added.

Amendment to the Specification

No new matter was added in the amendment to the specification. The specification was amended merely to correct a scribner's error in which Figure 39 was misidentified as Figure P11 in the amended paragraph.

Paragraphs 1 through 10 of the Office Action

Claims 1 through 20 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,982,771 to Caldara et al. in view of U.S. Patent No. 6,424,658 to Mathur.

Claims 1, 8 and 15 have each been amended to require that each interface receiver is associated with a unique pair of buffers so that each buffer pair only receives data from its associated interface receiver and that each buffer has a storage capacity less than the size of the incoming datagram. As stated on pages 55-56 of the specification, an advantage of embodiments set forth in the amended claims is to permit the handling of variably sized incoming packets in a manner unlike trivial dual input buffers and without the use of a third additional buffer (or more) in such a manner that a hardware reduction of the total chip area of the switch matrix/switch fabric component may be achieved.

In contrast, neither the Caldara reference nor the Mathur reference solve the problems answered by or provide the advantages provided by the embodiments claimed in amended claims 1, 8 and 15. Specifically, the Caldara reference utilizes more that a pair of buffers (*i.e.*, three or more buffers) to handle incoming data (see, *e.g.*, FIG. 1a, elements 132a, 132b and 132c of the Caldara reference) while the Mathur reference uses a pair of large capacity buffers (i.e., a pair of trivial

buffers) capable of containing an entire packet including 1.5 Kbit packets (see Mathur reference, column 6, lines 57-64).

The solutions suggested by Caldara and Mathur references totally teach away from the embodiments of the present invention claims in amended claims 1, 8 and 15 by requiring a hardware increase, and not a reduction, in the total chip area of the switch matrix/switch fabric component. There simply is no motivation in the Caldara and Mathur references (either separately or in combination) to enable, teach or suggest the solution provided in amended claims 1, 8, and 15 for storing an incoming datagram in a switch matrix of a switch fabric. Therefore, it is respectfully submitted that claims 1, 8 and 15, as amended, are patentably allowable over the Caldara and Mathur references. Because claims 2-7 depend from amended claim 1, claims 9-14 depend from amended claim 8, and claims 16-20 depend from amended claim 15, claims 2-7, 9-14, and 16-20 are now believed to be in condition for allowance by virtue of their dependency. Thus, for at least the foregoing reasons, reconsideration and withdrawal of the above rejection is respectfully requested.

New claims 21 has been added to further clarify and define the scope of embodiments of the claimed invention and is believed to be allowable.

If for any reason an insufficient fee has been paid, the Examiner is hereby authorized to charge the insufficiency to Deposit Account No. **05-0150**.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (650) 843-3215.

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